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<input type="checkbox"/>	L9	L7 and L2	24
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<input type="checkbox"/>	L8	L7	0
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<input type="checkbox"/>	L7	L6 and (pausing or pause)	130
<input type="checkbox"/>	L6	L3 and program counter and branch	1289
<input type="checkbox"/>	L5	L3 and context swap	37
<input type="checkbox"/>	L4	L3 and hop instruction	4
<input type="checkbox"/>	L3	micro-engine or micro engine or microengine or multiprocessor or multi processor or multi-processor or multiple processor	43757
		<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L2	L1 or 712/226-230.ccls.	4401
<input type="checkbox"/>	L1	717/124-133,149-161.ccls.	2915

END OF SEARCH HISTORY

Search Results Results 1 - 10 of about 34 for **micro engine hop instruction** - 0.34 sec. (About this page)

1. [http://www.ixpintel.nntu.nnov.ru/dokym\\_rykov/prim\\_kod\\_ixp1200/pdf/ReferenceDesign%20Microengine.pdf](http://www.ixpintel.nntu.nnov.ru/dokym_rykov/prim_kod_ixp1200/pdf/ReferenceDesign%20Microengine.pdf)  
... One per **Microengine**. Determine which Transmit Queues have packets ... Lookup next **hop** address. U  
move packet from FIFO to packet buffer ...  
ixpintel.nntu.nnov.ru/dokym\_rykov/prim\_kod\_ixp1200/pdf/... - 348k - [View as html](#) - [More from this site](#)
2. [DiffServ over Network Processors: Implementation and Evaluation \(PDF\)](#)   
... 2K **instruction** headroom (named "control store") for each **microengine** ... Mouftah, "Performance Eval  
[www.hoti.org/archive/hoti10/program/Lin\\_DiffServoverNP.pdf](http://www.hoti.org/archive/hoti10/program/Lin_DiffServoverNP.pdf) - 659k - [View as html](#) - [More from this site](#)
3. [Network Processors \(IXP 2400\) \(PDF\)](#)   
... can supply **instruction** source operands; when NN register is ... **microengine**, and each **microengine** t  
along with their next **hop** information ...  
[slatdb.freesevers.com/download/re\\_cs\\_np.pdf](http://slatdb.freesevers.com/download/re_cs_np.pdf) - 132k - [View as html](#) - [More from this site](#)
4. [Network processors: Guiding design through analysis \(PDF\)](#)   
... engine, which looks up the. next-**hop** IP address, classifies the packet or ... cycle shifter, an **instruction**-  
and 4 ...  
[www.cs.wisc.edu/~johnbent/Projects/net\\_proc.pdf](http://www.cs.wisc.edu/~johnbent/Projects/net_proc.pdf) - 243k - [View as html](#) - [More from this site](#)
5. [Intelligent Routing using Network Processors: Guiding Design through Analysis \(PDF\)](#)   
... engine, which looks up the. next-**hop** IP address, classifies the packet or ... cycle shifter, an **instruction**-  
and 4 ...  
[www.cs.wisc.edu/~kosart/papers/netproc.pdf](http://www.cs.wisc.edu/~kosart/papers/netproc.pdf) - 239k - [View as html](#) - [More from this site](#)
6. [NPU software taps virtual machine approach](#)   
However, the very strength of network processors — being a "soft" solution via software — is also the key  
new **instruction**-set architecture, address different ... packets, doing next-**hop** lookups on another set ... a  
per **microengine** ...  
[www.commsdesign.com/printableArticle?articleID=17602639](http://www.commsdesign.com/printableArticle?articleID=17602639) - 10k - [Cached](#) - [More from this site](#)
7. [http://www.ixpintel.nntu.nnov.ru/dokym\\_rykov/proc\\_ixp1200/pdf/StrongARMCore.ppt](http://www.ixpintel.nntu.nnov.ru/dokym_rykov/proc_ixp1200/pdf/StrongARMCore.ppt) (MIC  
... 16K B. **Instruction**. Cache. 8 K B ... StrongARM Core has access to all **Microengine** LOCAL\_CSRs ...  
Microengines (**hop** = step from one context change ...  
[ixpintel.nntu.nnov.ru/dokym\\_rykov/proc\\_ixp1200/pdf/StrongARMCore.ppt](http://ixpintel.nntu.nnov.ru/dokym_rykov/proc_ixp1200/pdf/StrongARMCore.ppt) - 98k - [View as html](#) - [More from](#)
8. [CommsDesign - NPU software taps virtual machine approach](#)   
High-level functional language let's designers express a wide variety of packet-processing applications. ...  
different ... packets, doing next-**hop** lookups on another set ... a thousand per **microengine**), eight hardwa  
[commsdesign.com/design\\_library/cd/np/showArticle.jhtml?...](http://commsdesign.com/design_library/cd/np/showArticle.jhtml?articleID=17602639) - 48k - [Cached](#) - [More from this site](#)
9. [EE Times -NPU software taps virtual machine approach](#)   
... have a new **instruction**-set architecture, address different ... packets, doing next-**hop** lookups on another  
threads per **microengine** ...  
[www.eetimes.com/in\\_focus/embedded\\_systems/OEG20040209S0036](http://www.eetimes.com/in_focus/embedded_systems/OEG20040209S0036) - 56k - [Cached](#) - [More from this site](#)
10. <http://www.gigascale.org/mescal/forum/81/mel.ppt> (MICROSOFT POWERPOINT)   
... memory lookups (4 threads per **microengine**) Currently no support ... processor, 128Kbyte L1 data and

latency per hop of 550  $\square$ sec ...

[www.gigascale.org/mescal/forum/81/mel.ppt](http://www.gigascale.org/mescal/forum/81/mel.ppt) - 675k - [View as html](#) - [More from this site](#)

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### Fresh Patents-Hop method for stepping parallel hardware threads ...

... The controller logic 72 includes in **instruction** decoder 73 ... capable of executing within the **microengine** 502d. **Hop** code is used in debugging the **microengine** 502d ...

www.freshpatents.com/Hop-method-for-stepping-parallel-hardware-threads-dt20041014ptan20040205719.php - 27k - [Cached](#) - [Similar pages](#)

### [PDF] G22.2243-001 High Performance Computer Architecture Outline

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... kind of packet, firewalling • Forwarding – Next **hop** (for routers ... 1.4GHz “**Microengine**” (custom ISA – no FP, division; 4K ... Special **instruction** set tuned ...

www.cs.nyu.edu/courses/fall04/G22.2243-001/lectures/lect14-2up.pdf - [Similar pages](#)

### [PDF] Microsoft PowerPoint - MicroTut1102.ppt

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... **Microengine** Array ... for support for ARM's ARM's thumb instructions thumb instructions ... enhancements to the **instruction** set enhancements to the **instruction** set ...

www.arl.wustl.edu/~pcrowley/raj.pdf - [Similar pages](#)

### [PDF] Intel Internet Exchange Architecture Portability Framework

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... Designers must not rely on the absence or characteristics of any features or instructions marked “reserved” or ... 19 2.1.1 **Microengine** Assembler Dispatch ...

www-2.cs.cmu.edu/.../course/18/544/www/extern/Software\_Framework/IXA-SDK/FrameworkRefManual.pdf - [Similar pages](#)

### [PDF] A Case for Asynchronous Microengines for Network Processing

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... the “ttl”, look- up the next **hop** destination IP ... Figure 5. Block diagram of IP Header Processing **Microengine** ... and jumps to mi-15(done) micro- **instruction**. ...

www.ece.northwestern.edu/EXTERNAL/anchor/final\_manuscripts/paper\_9.pdf - [Similar pages](#)

### Network Processor Building Blocks for All-IP Wireless Networks

... The **byte\_align instruction** allows concatenation of data ... is addressable storage located in the **microengine**. ... with their associated next-**hop** forwarding information ...

developer.intel.com/technology/itj/2002/volume06issue03/art08\_processorbuildingblocks/p04\_rncnodes.htm - 60k - [Cached](#) - [Similar pages](#)

### [PPT] Mescal Driver Applications

File Format: Microsoft Powerpoint 97 - [View as HTML](#)

... processor, 128Kbyte L1 data and **instruction** caches, 1Mbyte ... encryption routines were added to each receive **microengine**. ... required maximum latency per **hop** of 550 ...

www.gigascale.org/mescal/forum/81/mel.ppt - [Similar pages](#)

### [PPT] Introduction to Network Processors

File Format: Microsoft Powerpoint 97 - [View as HTML](#)

... Applications: IPv4 Routing. Routers determine next **hop** and forward packets. ... IXP1200 **Microengine**. 4 hardware contexts. ... 4KB SRAM **instruction** stor – not a cache! ...

www.cs.ucr.edu/~bhuyan/CS260/LECTURE1.ppt - [Similar pages](#)

[PDF] [IP: Addresses and Forwarding](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... 1000 1996 1997 1998 1999 2000 2001 CPU Instructions per minimum length packet since

1996 ... IP Address Next Hop Queue ... Fine-grained parallelism: **instruction-level** ...

[www.ecse.rpi.edu/Homework/shivkuma/teaching/sp2004/ip2004-router-design.pdf](http://www.ecse.rpi.edu/Homework/shivkuma/teaching/sp2004/ip2004-router-design.pdf) - [Similar pages](#)

[PDF] [02-237 Teja L3\(IPv4\)v2TST](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

... 1 always resolves the 'Next-Hop' route in ... languages for the StrongARM and **microengine** processors, the ... Plane microcode Receive: 472 instructions store size ...

[www.teja.com/content/teja\\_IPv4.pdf](http://www.teja.com/content/teja_IPv4.pdf) - [Similar pages](#)

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Terms used **multiprocessor hop microengine**

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**1 [Hardware support for distributed objects in a hypercube](#)**

J. L. Kozarek

January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

Full text available: pdf(813.20 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A survey of parallel programs written for an experimental hypercube indicates that while systolic dataflow programs map well to a hypercube, general purpose programs with random dataflow are seriously constrained by the cost of communication. This paper proposes the augmentation of the hypercube architecture with a special-purpose communications coprocessor that provides hardware support for distributed objects. We anticipate this will increase the efficiency of inter-process commun ...

**2 [The design of nectar: a network backplane for heterogeneous multicomputers](#)**

Emmanuel Arnould, H. T. Kung, Francois Bitz, Robert D. Sansom, Eric C. Cooper

April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems, Volume 17 Issue 2**

Full text available: pdf(1.73 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Nectar is a "network backplane" for use in heterogeneous multicomputers. The initial system consists of a star-shaped fiber-optic network with an aggregate bandwidth of 1.6 gigabits/second and a switching latency of 700 nanoseconds. The system can be scaled up by connecting hundreds of these networks together. The Nectar architecture provides a flexible way to handle heterogeneity and task-level parallelism. A wide variety of machines can be connected as Nectar nodes ...

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#### 1 Asynchronous microengines for efficient high-level control

*Jacobson, I.; Gopalakrishnan, G.;*

Advanced Research in VLSI, 1997. Proceedings., Seventeenth Conference on , 16 Sept. 1997

Pages:201 - 218

[\[Abstract\]](#)   [\[PDF Full-Text \(1220 KB\)\]](#)   IEEE CNF

#### 2 The effect of frequency on the lifetime of a surface micromachined microengine driving a load

*Tanner, D.M.; Miller, W.M.; Eaton, W.P.; Irwin, L.W.; Peterson, K.A.; Dugger, Senft, D.C.; Smith, N.F.; Tangyunyong, P.; Miller, S.L.;*

Reliability Physics Symposium Proceedings, 1998. 36th Annual. 1998 IEEE International , 31 March-2 April 1998

Pages:26 - 35

[\[Abstract\]](#)   [\[PDF Full-Text \(2692 KB\)\]](#)   IEEE CNF

#### 3 Surface-micromachined gear trains driven by an on-chip electrostatic microengine

*Sniegowski, J.J.; Garcia, E.J.;*

Electron Device Letters, IEEE , Volume: 17 , Issue: 7 , July 1996

Pages:366 - 368

[\[Abstract\]](#)   [\[PDF Full-Text \(612 KB\)\]](#)   IEEE JNL

#### 4 MEMS reliability in a vibration environment

*Tanner, D.M.; Walraven, J.A.; Helgesen, K.S.; Irwin, L.W.; Gregory, D.L.; Sta J.R.; Smith, N.F.;*

Reliability Physics Symposium, 2000. Proceedings. 38th Annual 2000 IEEE

International , 10-13 April 2000  
Pages:139 - 145

[\[Abstract\]](#) [\[PDF Full-Text \(840 KB\)\]](#) IEEE CNF

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**5 Pin-j int design effect on the reliability f a p lysilic n microengine**  
*Tanner, D.M.; Walraven, J.A.; Mani, S.S.; Swanson, S.E.;*  
Reliability Physics Symposium Proceedings, 2002. 40th Annual , 7-11 April 200  
Pages:122 - 129

[\[Abstract\]](#) [\[PDF Full-Text \(757 KB\)\]](#) IEEE CNF

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**6 The effect of humidity on the reliability of a surface micromachined microengine**  
*Tanner, D.M.; Walraven, J.A.; Irwin, L.W.; Dugger, M.T.; Smith, N.F.; Eaton, Miller, W.M.; Miller, S.L.;*  
Reliability Physics Symposium Proceedings, 1999. 37th Annual. 1999 IEEE International , 23-25 March 1999  
Pages:189 - 197

[\[Abstract\]](#) [\[PDF Full-Text \(2124 KB\)\]](#) IEEE CNF

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**7 Effect of W coating on microengine performance**  
*Mani, S.S.; Fleming, J.G.; Walraven, J.A.; Sniegowski, J.J.; se Beer, M.P.; Irw L.W.; Tanner, D.M.; LaVan, D.A.; Dugger, M.T.; Jakubczak, J.; Miller, W.M.;*  
Reliability Physics Symposium, 2000. Proceedings. 38th Annual 2000 IEEE International , 10-13 April 2000  
Pages:146 - 151

[\[Abstract\]](#) [\[PDF Full-Text \(672 KB\)\]](#) IEEE CNF

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**8 Fluidic packaging of microengine and microrocket devices for high-pressure and high-temperature operation**  
*Peles, Y.; Srikar, V.T.; Harrison, T.S.; Protz, C.; Mracek, A.; Spearing, S.M.;*  
Microelectromechanical Systems, Journal of , Volume: 13 , Issue: 1 , Feb. 200  
Pages:31 - 40

[\[Abstract\]](#) [\[PDF Full-Text \(736 KB\)\]](#) IEEE JNL

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**9 Intelligent peripheral modules for microcontrollers**  
*Melear, C.;*  
Southcon/95. Conference Record , 7-9 March 1995  
Pages:90 - 99

[\[Abstract\]](#) [\[PDF Full-Text \(632 KB\)\]](#) IEEE CNF

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**10 HPSm2: A refined single-chip microengine**  
*Hwu, W.W.; Patt, Y.N.;*  
System Sciences, 1988. Vol.I. Architecture Track, Proceedings of the Twenty-F Annual Hawaii International Conference on , Volume: 1 , 5-8 Jan. 1988  
Pages:30 - 40

[\[Abstract\]](#) [\[PDF Full-Text \(756 KB\)\]](#) IEEE CNF



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**11 Application-specific programmable control for high-performance asynchronous circuits**

*Jacobson, H.M.; Gopalakrishnan, G.;*

Proceedings of the IEEE , Volume: 87 , Issue: 2 , Feb. 1999

Pages:319 - 331

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) [IEEE JNL](#)

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**12 Bent-beam electrothermal actuators-Part II: Linear and rotary microengines**

*Jae-Sung Park; Chu, L.L.; Oliver, A.D.; Gianchandani, Y.B.;*

Microelectromechanical Systems, Journal of , Volume: 10 , Issue: 2 , June 200

Pages:255 - 262

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) [IEEE JNL](#)

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**13 Radiation effects on surface micromachined comb drives and microengines**

*Schanwald, L.P.; Schwank, J.R.; Sniegowski, J.J.; Walsh, D.S.; Smith, N.F.;*

*Peterson, K.A.; Shaneyfelt, M.R.; Winokur, P.S.; Smith, J.H.; Doyle, B.L.;*

Nuclear Science, IEEE Transactions on , Volume: 45 , Issue: 6 , Dec. 1998

Pages:2789 - 2798

[\[Abstract\]](#) [\[PDF Full-Text \(1204 KB\)\]](#) [IEEE JNL](#)

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**14 Development of Si-SiC hybrid structures for elevated temperature micro-turbomachinery**

*Hyung-Soo Moon; Dongwon Choi; Spearing, S.M.;*

Microelectromechanical Systems, Journal of , Volume: 13 , Issue: 4 , Aug. 200

Pages:676 - 687

[\[Abstract\]](#) [\[PDF Full-Text \(2288 KB\)\]](#) [IEEE JNL](#)

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**15 An electrostatic, on/off microvalve designed for gas fuel delivery for the MIT microengine**

*Xue'en Yang; Holke, A.; Jacobson, S.A.; Lang, J.H.; Schmidt, M.A.; Umans, S.;*

Microelectromechanical Systems, Journal of , Volume: 13 , Issue: 4 , Aug. 200

Pages:660 - 668

[\[Abstract\]](#) [\[PDF Full-Text \(1832 KB\)\]](#) [IEEE JNL](#)

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[Chapter 2 The Ixp12xx Programming Environment - The Goal Of](#) (Correct)

compiler. What you discovered was that the **microengines** don't run any operating systems, and the C StrongARM\* core{ XE "StrongARM core" and six **microengines** all on the same die. The StrongARM core is an [www.intel.com/intelpress/ixp1200/ixp-chapter.pdf](http://www.intel.com/intelpress/ixp1200/ixp-chapter.pdf)

[Performance Analysis of the Intel IXP1200 Network Processor - Http](#) (Correct)

and six programmable RISC cores (also known as **microengines**) The core runs the VxWorks operating system the VxWorks operating system and controls the **microengine** threads. Each **microengine** can execute up to core uses these registers to program, control, and **debug** the **microengines**. Each **microengine** instruction is [gs129.sp.cs.cmu.edu/papers/15740f00-ixp1200.ps](http://gs129.sp.cs.cmu.edu/papers/15740f00-ixp1200.ps)

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